Listing of Claims

1. (~~Previously~~ Presently Amended) A data storage device comprising:

an array of resistive memory cells having rows and columns;

a set of diodes electrically connected in series to a plurality of memory cells in the array;

a plurality of word lines extending along the rows of the array;

a plurality of bit lines extending along the columns of the array;

a first selected memory cell in the array, wherein the first selected memory cell is positioned between a first word line in the plurality of word lines and a first bit line in the plurality of bit lines; and

a circuit electrically connected to the array and capable of monitoring a signal current flowing through the first selected memory cell and comparing the signal current to an average reference current in order to determine which of a first resistance state and a second resistance state the first selected memory cell is in[.];

wherein the circuit is capable of obtaining the average reference current by placing an unselected memory cell in a first resistance state, sensing a first reference current while the unselected memory cell is in the first resistance state, placing the unselected memory cell in a second resistance state, sensing a second reference current while the unselected memory cell is in the second resistance state, and averaging the first reference current and the second reference current to obtain the average reference current.

2. (Previously Deleted) The device of claim 1, wherein the array of resistive memory cell comprises a magnetic random access memory (MRAM) cell.

3. (Previously Deleted) The device of claim 2, wherein the MRAM memory cell comprises a tunnel junction.

4. (Previously Deleted) The device of claim 1, wherein the set of diodes comprises a thin-film diode.

5. (Previously Deleted) The device of claim 1, further comprising a second selected memory cell in the array, wherein the first selected memory cell is in a first layer of the array and wherein the second selected memory cell is in a second layer of the array.

6. (Previously Deleted) The device of claim 1, wherein the circuit is capable of obtaining the average reference current by placing the first selected memory cell in the first resistance state, sensing a first reference current while the first selected memory cell is in the first resistance state, placing the first selected memory cell in the second resistance state, sensing a second reference current while the first selected memory cell is in the second resistance state, and averaging the first reference current and the second reference current to obtain the average reference current.

7. (Previously Deleted) The device of claim 6, wherein the circuit is capable of returning the first selected memory cell to an original resistance state wherein the first selected memory cell has the signal current flowing there through.

8. (Previously Deleted) The device of claim 1, wherein the circuit is capable of obtaining the average reference current from an externally supplied source.

9. (Presently Amended) The device of claim 1, wherein the circuit is capable of obtaining the average reference current <u>using a triple sample counter for determining the first reference current and the second reference current</u> [by monitoring memory cells other than the first selected memory cell].

10. (Previously Deleted) The device of claim 1, wherein the circuit is capable of writing to the first selected memory cell by applying sufficient energy to the first word line and the first bit line to transform the first selected memory cell from a first resistance state to a second resistance state.

11. (Presently Amended) A method of sensing a resistance state of a first selected memory cell in a data storage device that includes an array of resistive memory cells, a plurality of word lines extending along rows of the array, a plurality of bit

lines extending along columns of the array, a first selected memory cell in the array, wherein the first selected memory cell is positioned between a first word line in the plurality of word lines and a first bit line in the plurality of bit lines, and a circuit electrically connected to the array, the method comprising:

providing a set of diodes electrically connected in series to a plurality of memory cells in the array;

placing a first unselected memory cell in a first resistance state;

sensing a first reference current while the unselected memory cell is in the first resistance state;

placing the unselected memory cell in a second resistance state;

sensing a second reference current while the unselected memory cell is in the second resistance state; and

averaging the first reference current and the second reference current to obtain a value for the average reference current;

sensing a signal current flowing through the first selected memory cell with the array;

comparing the signal current to an average reference current; and

determining which of a first resistance state and a second resistance state the first selected memory cell is in by comparing the signal current to the reference current.

12. (Previously Deleted) The method of claim 11, wherein the providing step comprises providing a set of thin-film diodes.

13. (Previously Deleted) The method of claim 11, wherein the sensing step comprises sensing the signal current flowing through an magnetic random access memory (MRAM) cell.

14. (Previously Deleted) The method of claim 11, wherein the sensing step comprises sensing the signal current flowing through the MRAM memory cell that includes a tunnel junction.

15. (Previously Deleted) The method of claim 14, wherein the determining step comprises determining which of an anti-parallel ferromagnetic state and a parallel ferromagnetic state the MRAM memory cell is in.

16. (Previously Deleted) The method of claim 11, further comprising obtaining the average reference current from an externally supplied source.

17. (Presently Amended) The method of claim 11, further comprising obtaining the average reference current by using a triple sample counter for determining the first reference current and the second reference current .[monitoring cells other than the first selected memory cell.]

18. (Previously Deleted) The method of claim 11, further comprising:

placing the first selected memory cell in the first resistance state;

sensing a first reference current while the first selected memory cell is in the first resistance state;

placing the first selected memory cell in the second resistance state;

sensing a second reference current while the first selected memory cell is in the second resistance state; and

averaging the first reference current and the second reference current to obtain a value for the average reference current.

19. (Previously Deleted) The method of claim 18, further comprising returning the first selected memory cell to the state that the first selected memory cell was in before the first reference current and the second reference current were sensed.

20. (Previously Deleted) The method of claim 11, further comprising sensing a signal current flowing through a second selected memory cell positioned in a different layer of the array than where the first selected memory cell is positioned.